REMARKS

Claims 1-5 are presently pending in the application. Reconsideration and allowance of all claims are respectfully requested in view of the following remarks.

The Examiner has objected to Fig. 5 of the drawings, stating that Fig. 5 should be designated by a legend such as --Prior Art--.

The Examiner is respectfully requested to acknowledge receipt of one (1) sheet of Proposed Drawing Corrections which amends Fig. 5 to add the legend --Prior Art--. Corrected formal drawings will follow in due course.

The Examiner has rejected Claim 1 under 35 U.S.C. §102(b) as being anticipated by Shiraishi. Claim 4 was rejected by the Examiner under 35 U.S.C. §103 as being unpatentable over Shirarishi. However, the Examiner has found Claims 2, 3, and 5 allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims. Claims 2 and 5 have been rewritten into independent form, which should result in the immediate allowance of Claims 2, 3, and 5. For the following reasons, the prior art rejections are respectfully traversed.

The Applicant respectfully submits that Shiraishi does not teach or suggest a semiconductor device including a plurality of active region formed on a chip, the active regions being separated from one another by a boundary region; and a plurality of logic circuits having either one of the same functions and different functions being mounted in each of the active regions, as recited in amended Claim 1.

Rather, Shiraishi is silent with respect to a boundary region separating the active regions and the plurality of logic circuits.

Accordingly, Claim 1 is not anticipated by Shiraishi, and the rejection of Claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Further, since Claim 4 depends from Claim 1, it is also patentably distinguishable over Shiraishi

for the reasons cited above with respect to Claim 1.

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 19-3140.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, the fifth paragraph was amended as follows:

Each of the input/output pads 22 is typically shaped to have a square with a side of approximately 100 [im] μm. Due to limitations of mechanical accuracy of a bonding apparatus for use in a wire bonding process, it is difficult to significantly reduce the input/output pads 22 in size. Thus, when the required number of input/output pads 22 are arranged in the periphery of the rectangular chip 20 as shown in Fig. 5, the minimum chip size is accordingly determined.

Page 2, the second paragraph was amended as follows:

With an increasingly miniaturized LSI, a higher speed processing ability, and realization of an extremely large-scale integrated circuit in a very limited area on a chip, however, the overall active region 21 may not be filled with circuits. In this case, the active region 21 includes [an] a no-patterned region which has no circuit mounted therein. [An] A no-patterned region may also occur for circuits that involve relatively simple signal processing and uses a small number of gates.

Page 2, the third paragraph was amended as follows:

For circuits that do not require high speed processing, occurrence of [an] a no-patterned region can be avoided by lowering its integration degree. For circuits that require high speed processing, however, a higher integration degree (miniaturization) is needed, and in this case, design must be performed in preparation for occurrence of [an] a no-patterned region. In addition, when [an] a no-patterned region occurs, a problem of too much waste arises since the no-patterned region cannot be effectively utilized.

Page 2, the fifth paragraph, continuing to page 3, was amended as follows:

In this manner, in a conventional LSI, since the minimum chip size is inevitably determined by the number and size of the input/output pads, a problem of [an] a no-patterned region created in an active region surrounded by an I/O region arises in a highly integrated circuit or a circuit with a small number of gates. Thus, there are challenges of solving such a problem and improving the yield of a semiconductor device.

Page 3, the second full paragraph was amended as follows:

In the semiconductor device thus configured, [an] a no-patterned region having no circuit mounted therein is utilized in the active region where circuits can be mounted, and a plurality of logic circuits having functions identical to or different from those of logic circuits mounted in the remaining active region is mounted in the no-patterned region. Consequently, the device can be shipped as a product if at least one of the logic circuits operates normally to significantly improve and more effectively utilize the semiconductor device.

Page 4, the seventh full paragraph, continuing to page 5, was amended as follows:

Arranged in the I/O region 12 are a plurality of input/output pads 14 which are electrodes for connecting lead-out terminals for a logic LSI with a circuit inside the semiconductor chip through bonding wire. Each of the input/output pads 14 is shaped to have a square with a side of approximately 100 [im] μm.

Page 5, the first full paragraph was amended as follows:

A hatched portion in Fig. 1 is [an] a no-patterned region 13 where no circuit is mounted if only one logic circuit block is mounted in the active region 11 surrounded by the I/O region 12.

Page 5, the third full paragraph was amended as follows:

As shown in Fig. 2, a portion of the no-patterned region shown in Fig. 1 is defined as a boundary region 15, and regions on both sides of the boundary region 15 are defined as a first active region 16 and a second active region 17, respectively. In the second active region 17, circuits having the same functions as, or circuits having different functions from, circuits mounted in the first active region 16, are mounted. It should be noted that the area of the first active region 16 may or may not be equal to the area of the second active region 17.

Page 7, the fourth full paragraph, continuing to page 8, was amended as follows:

Conversely, when the signal SEL is set to HIGH level, since both the P-channel transistor T_{pa} and N-channel transistor T_{na} are turned off, neither power nor ground is supplied to the block A and thus, the block A does not operate. However, since both the P-channel transistor T_{pb} and N-channel transistor T_{nb} are turned on, power and ground are supplied to the block B, and thus the circuits constituting the block B [operates] <u>operate</u>.

Page 10, the sixth full paragraph, was amended as follows:

In addition, since [an] <u>a</u> no-patterned region on a semiconductor chip can be considerably reduced to effectively utilize a semiconductor constituting a substrate, the utilization ratio for a wafer is significantly increased.

Page 12, the first full paragraph was amended as follows:

To address this, since [an] <u>a</u> no-patterned region is created with an increasingly miniaturized LSI in an active region where a circuit can be mounted, the present invention effectively utilizes such a region, which conventionally has been [an] <u>a</u> no-patterned region, by mounting a redundant circuit there. Therefore, even when a portion of a logic circuit is defective, the redundant circuit is caused to function similarly thereto to allow improvement in the yield of the logic LSI.

IN THE CLAIMS:

The claims were amended as follows:

1. (Amended) A semiconductor device, comprising

an I/O region formed on a chip and having at least an input/output pad;

[an] a plurality of active region formed on said chip, said active regions being separated from one another by a boundary region;

a plurality of logic circuits having either one of the same functions [or] and different functions being mounted in each of said active [region] regions, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits.

2. (Amended) The semiconductor device [according to claim 1,] comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a disconnecting section, and

said disconnecting section is disconnected to allow permanent setting of an operable circuit.

4. (Amended) The semiconductor device according to claim 1, wherein said selection circuit selects a logic circuit to be operated on [the] a basis of a signal input supplied from [the] an outside through said input/output pad.

5. (Amended) The semiconductor device [according to claim 1,] comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a transistor element connected in series with each said logic circuit between said logic circuit and a power terminal, and

said transistor element selects a logic circuit to be operated on [the] a basis of a signal input supplied from [the] an outside through said input/output pad.

IN THE ABSTRACT OF THE DISCLOSURE:

The title was amended as follows:

[ABSTRUCT] ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure was amended as follows:

A semiconductor device includes [In a conventional LSI, since a minimum chip size is inevitably determined by the number and size of input/output pads formed on a chip, an no-patterned region occurs in an active region surrounded by an I/O region in a highly integrated circuit or a circuit with a small number of gates. The present invention intends to solve this problem to improve a semiconductor device. In a semiconductor device comprising] on the same chip at least an I/O region where an input/output pad is formed and active regions where a circuit can be mounted, where a plurality of logic circuits having the same functions or different functions are mounted in the active regions on the same chip.